

Application No. 10/016,540
Filed: October 26, 2001
TC Art Unit: 2182
Confirmation No.: 7896

REMARKS

The instant Remarks are filed in response to the official action dated June 10, 2004. Reconsideration is respectfully requested.

The status of the claims is as follows:

Claims 1-14 are currently pending.

Claims 1-14 stand rejected.

The Examiner has rejected base claim 8 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Specifically, the official action indicates that the limitation "the parallel data" recited in claim 8 has insufficient antecedent basis. The Applicants respectfully submit, however, that the antecedent basis for the limitation "the parallel data" is provided in the preamble of claim 8, which recites, in relevant part, "a system for transmitting parallel data to a destination". Claim 8 then recites in the body of the claim the step of "segregating the parallel data into a plurality of parallel data words, each parallel data word comprising a plurality of data bits". Because sufficient antecedent basis is provided for the limitation "the parallel data" in the preamble of claim 8, the Applicants

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respectfully submit that the rejection of base claim 8 under section 112 of the Patent Laws is unwarranted and should be withdrawn.

The Examiner has rejected claims 1-6 and 8-14 under 35 U.S.C. 103(a) as being unpatentable over Ducaroir *et al.* (USP 6,167,077) in view of Hogeboom (USP 6,262,998). Specifically, as to claim 1, the official action indicates that the Ducaroir reference teaches substantial features of the method of transmitting parallel data to a destination over a plurality of serial data lines, but fails to teach transmitting a clock signal to the destination over a clock line in parallel with the plurality of serial data lines, the clock signal having at least one data bit of each parallel data word encoded thereon, and aligning the regenerated parallel data words using the respective data bits encoded on the clock signal. The official action further indicates that the Hogeboom reference teaches transmitting a clock signal to the destination over a clock line in parallel with the plurality of serial data lines, the clock signal having at least one data bit of each parallel data word encoded thereon, and aligning the regenerated parallel data words using the respective data bits encoded on the clock signal. The Applicants respectfully submit, however, that the suggested combination of the Ducaroir and Hogeboom references

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does not describe the limitations of each and every step of base claim 1, and therefore the suggested combination does not render claim 1 and the claims dependent therefrom obvious.

For example, Hogeboom fails to disclose transmitting a clock signal to a destination over a clock line in parallel with a plurality of serial data lines, in which the clock signal has at least one data bit of each parallel data word encoded thereon, as recited in base claim 1. Hogeboom also fails to disclose aligning regenerated parallel data words using the respective data bits (*i.e.*, the at least one data bit of each parallel data word) encoded on the clock signal, as recited in claim 1.

Instead, Hogeboom merely discloses a single integrated signal path carrying both synchronous clock information and control data (see column 2, lines 3-5, of Hogeboom). Hogeboom further discloses that an alternate edge of the clock signal is independently modulated in increments of one data bit time to carry the control data, and that the control data may be used for low speed timing purposes such as framing (see column 2, lines 32-37, of Hogeboom). However, Hogeboom discloses nothing about encoding at least one data bit of each parallel data word onto the clock signal, and using these data bits encoded on the clock

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signal for aligning the regenerated parallel data words, as recited in base claim 1.

This is clearly shown by Hogeboom's description of a high speed data bus structure, as depicted in Fig. 4 of the Hogeboom reference. Specifically, Hogeboom indicates that the high speed data structure includes an encoder functional block 400 that receives high speed data along with control information to be transmitted. The encoder functional block 400 transmits the high speed data over a pathway 404. Hogeboom further indicates that the encoder functional block 400 generates clock information and combines the clock information with the control information for subsequent transmission over a pathway 406 (see column 4, lines 43-53, and Fig. 4, of Hogeboom). Hogeboom therefore describes three types of data or information that is transmitted from the encoding functional block 400 to a decoding functional block 402 over the pathways 404 and/or 406, namely, the high speed data, the control information, and the clock information. The Applicants respectfully submit that the Hogeboom reference provides no teaching or suggestion that the control information transmitted over the pathway 406 includes at least one bit of the high speed data transmitted over the pathway 404. In fact, the Hogeboom reference provides no description whatsoever of what constitutes

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the control information or of how the control information is derived.

It is well settled that to consider subject matter "as a whole" under section 103 of the Patent Laws affirmatively involves taking into account all of the limitations of a claim. Because the Hogeboom reference fails to disclose the limitations that the clock signal has at least one data bit of each parallel data word encoded thereon, and that the regenerated parallel data words are aligned using the respective data bits of the parallel data words encoded on the clock signal, as recited in base claim 1, the suggested combination of the Ducaroir and Hogeboom references does not render base claim 1 and the claims dependent therefrom obvious. Accordingly, the Applicants respectfully submit that the rejections of claims 1-6 under 35 U.S.C. 103 are unwarranted and should be withdrawn.

Because base claim 8 recites a system for transmitting parallel data to a destination that includes a plurality of parallel to serial converters for converting protocol data to a clock signal having the at least one data bit of each parallel data word encoded thereon, and a de-skew circuit for aligning regenerated parallel data words using the at least one data bit of each parallel data word included in the protocol data, the

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Applicants respectfully submit that, for at least the reasons outlined above with respect to claim 1, the suggested combination of the Ducaroir and Hogeboom references does not render base claim 8 and the claims dependent therefrom obvious. Accordingly, the Applicants respectfully submit that the rejections of claims 8-14 under 35 U.S.C. 103 are unwarranted and should be withdrawn.

The Examiner has rejected dependent claim 7 under 35 U.S.C. 103(a) as being unpatentable over Ducaroir and Hogeboom in view of Lecourtier et al. (USP 6,560,275). The Applicants respectfully submit, however, that the Lecourtier reference does not cure the deficiencies of the Ducaroir and Hogeboom references, and therefore the suggested combination of the Ducaroir, Hogeboom, and Lecourtier references does not render dependent claim 7 obvious. Accordingly, the Applicants respectfully submit that the rejection of claim 7 under section 103 of the Patent Laws is unwarranted and should be withdrawn.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of

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the present application.

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